SPECIFICATION

1. Title of the Invention

SOLID STATE IMAGE PICK-UP DEVICE

2. What is claimed is:

1. A solid state image pick-up device comprising:

a plurality of photoelectric conversion devices arranged two-dimensionally;

a vertical switching MOS transistor transmitting detecting signals of the photoelectric conversion devices;

a vertical signal line;

a horizontal switching MOS transistor;

a horizontal signal line;

vertical and horizontal scanning circuits sequentially applying scanning pulses to each gate electrode of the vertical and horizontal switching MOS transistors; and

a preamplifier amplifying a signal output from the horizontal signal line, wherein rectangular waveform pulse of a horizontal period is added to the output of the preamplifier to remove black level offset.

2. A solid state image pick-up device comprising:

a plurality of photoelectric conversion devices arranged two-dimensionally;

a vertical switching MOS transistor transmitting detecting signals of the photoelectric conversion devices;

a vertical signal line;

a horizontal switching MOS transistor;

a horizontal signal line; and

vertical and horizontal scanning circuits sequentially applying scanning pulses to each gate electrode of the vertical and horizontal switching MOS transistors, wherein the horizontal signal line is separated by a MOS transistor A, source and drain of the MOS transistor A are diffused on a well separated from other portions and the MOS transistor A is switched at a part of a horizontal flyback period, thereby removing black level offset.

3. A solid state image pick-up device comprising:

a plurality of photoelectric conversion devices arranged two-dimensionally;

a vertical switching MOS transistor transmitting a detecting signal of the photoelectric conversion devices;

a vertical signal line;

a coupling circuit;

a horizontal transmitting charge coupled device; and

a vertical scanning circuit sequentially applying scanning pulses to a gate electrode of the vertical switching MOS transistor, wherein a means for adjusting a part of a horizontal flyback period with a voltage is provided at the output of the charge coupled device, thereby removing black level offset.

3. Detailed Description of the Invention

The present invention relates to a solid state image pick-up device that reads optical data stored in a plurality of photodiodes arranged two-dimensionally on a surface of a semiconductor substrate. Particularly, the present invention relates to a solid state image pick-up device that stabilizes black balance.

A related art solid state image pick-up device will be described with reference to FIG. 1 to FIG. 4.

FIG. 1 illustrates an example of a two-dimensional solid state image pick-up device, and FIG. 2 illustrates an example of a timing chart of horizontal and vertical scanning pulses. Referring to FIG. 1, reference numerals 1 and 2 denote horizontal and vertical scanning circuits, respectively. The horizontal and vertical scanning circuits apply clock pulses CP_H and CP_V of two to four images so that output pulse rows $O_H(1)$, $O_H(2)$, ..., $O_V(1)$, $O_V(2)$... shown in FIG. 2 shifted during a certain clock timing period may be output to output lines of respective stages of the scanning circuits by start pulses SP_H and SP_V. Switching devices 6 and 7 are sequentially switched by the pulse rows so that the signals from each photoelectric conversion device 3 arranged two-dimensionally are fetched on a horizontal signal line 5. Since the signals from the photoelectric conversion devices correspond to optical images projected thereon, image signals can be fetched by the above operation.

In the aforementioned solid state image pick-up device, 500×500 photoelectric conversion devices, switching devices and scanning circuits are required to obtain high resolution. Therefore, MOS-LSI technology is used, which facilitates high integration and forms photoelectric conversion devices and switching devices in a single body. FIG. 3 illustrates a structure of a photoelectric

conversion portion that occupies almost all areas of a solid state image pick-up IC. Referring to FIG. 3, a reference numeral 20 denotes an n type semiconductor substrate, and 19 a P type well. Reference numerals 7 and 6 denote switches (hereinafter, referred to as "MOS transistors") consisting of insulating gate type electric field effect transistors for respectively selecting horizontal and vertical positions. The MOS transistors are comprised of n type diffusion layers 13, 14 and 15 constituting drain or source, and gate electrodes 16 and 17 formed by interposing an insulating oxide layer 18. A reference numeral 13 denotes a cathode of a photodiode 3 based on the source of the vertical MOS transistor 6.

Charges Q in proportion to incident light are filled in the cathode of the photodiode 3 of the vertical position through the vertical signal line 4. In this case, the output pulse $O_V(m)$ of the vertical scanning circuit 2 is applied to the gate of the MOS transistor 6. Subsequently, the charges Q are filled in the vertical signal line 4 of the horizontal position from a constant voltage power source 11. In this case, the output pulse $O_H(n)$ of the horizontal scanning circuit 1 is applied to the gate of the MOS transistor 7. The charged current is read out from a signal output terminal 8 as a video signal through a load resistor 12. The load resistor 12 means an input impedance of a voltage feedback type preamplifier.

FIG. 4 illustrates a flow of signal charges that are channel potentials at each time period of t_1 to t_5 shown in FIG. 2. Since n channel devices are provided, the potentials are forwarded downwardly. A reference numeral 21 denotes a cathode of a photodiode, 22 a vertical signal line, 23 a horizontal signal line, 24 and 25 vertical and horizontal MOS switch barriers, and 30, which is marked by an oblique line, signal charges.

In FIG. 3, the constant voltage is applied to the well 19 due to blooming. In case of no blooming, the signal charges 30 are permeated into the vertical signal line 22 by passing through the barrier 24 when the charges are increased due to strong incident light to the photodiode. This is displayed on a monitor as the blooming in which a bright portion is hung up and down. In FIG. 3, nPn transistor T_r is comprised of the substrate 20, the well 19 and the cathode 13 of the photodiode by applying voltages V_{WPD} and V_{SUB} to the well 19 and the substrate 20. If the potential of the cathode 13 becomes less than the potential V_S which is higher than the barrier potential V_L generated when the vertical MOS transistor 6 is turned off, the transistor T_r is turned on so that surplus electrons may be escaped from the

cathode 13 to the substrate 20. For example, a well bias W_{WPD} of 0.7V and a substrate bias S_{VUB} of 7V are used in comparison with a video bias V_V of 3V and a scanning circuit output pulse voltage of 0V to 7V.

The related art solid state image pick-up device has a problem such as black level offset due to blooming. Hereinafter, black level offset will be described with reference to FIG. 5 to FIG. 8.

FIG. 5 illustrates a typical waveform of a video signal during a dark period. As shown in FIG. 5, more black signals are output to a horizontal scanning period H_{SC} than a horizontal flyback period H_{BL}.

FIG. 4 illustrates an equalizing circuit to the output of a preamplifier. It has been noted by a detailed review of inventors of this invention that currents I_{BH} and I_{BV} are applied below the gate of each MOS transistor by switching of the MOS transistors.

Such offset currents $I_B(=1B_H+1B_V)$ may be caused by a charge pumping phenomenon. The charge pumping phenomenon will be described with reference to FIG. 7.

FIG. 7 is a sectional view illustrating an example of an n channel MOS transistor. FIG. 7a illustrates the state that a pulse increasing from minus to plus is applied to a gate electrode 101. In this case, a channel is formed below the gate electrode 101, and electrons 106 are induced from diffusion layers 103 and 104 of source and drain. The source and the drain are conducted. FIG. 7b illustrates the state that the source and the drain are not conducted as the pulse applied to the gate electrode 101 descends. In FIG. 7a, the electrons 106 induced in the channel below the gate electrode 101 return to the diffusion layers 103 and 104. At this time, if the gate pulse descends rapidly, the electrons 106 may occur, which are trapped below the gate electrode 101 so as not to return to the diffusion layers. Such electrons 106 are absorbed in the substrate 105. This is called the charge pumping phenomenon. Consequently, the current from the substrate 105 is applied below the gate electrode 101 by switching.

FIG. 8 illustrates properties of the black level offset current I_B assumed to be caused by the charge pumping phenomenon. The offset current I_B increases in proportion to the well voltage V_{WPD}. When the well voltage V_{WPD} is 0.7V, the offset current I_B is 14nA that corresponds to considerable quantity in comparison with several hundreds of nA.

Particularly, in a color solid state image pick-up device, since white balance is adjusted before DC reproduction, black offset occurs differently per color. This does not maintain black balance and degrades picture quality.

An object of the present invention is to provide a color solid state image pick-up device that removes drawbacks of the related art and has stable black balance.

A main feature of the present invention is to remove black level offset from the output of the solid state image pick-up device or the preamplifier. To remove the black level offset, the followings can be suggested.

1) The rectangular pulse of the horizontal period is applied to the signal.

2) The charge pumping phenomenon intentionally occurs at a part of the horizontal flyback period.

3) The output level is adjusted at a part of the horizontal flyback period.

FIG. 9a is a circuit diagram illustrating a solid state image pick-up device according to one embodiment of the present invention. A rectangular waveform pulse (FIG. 9b) having a horizontal period and polarity opposite to that of the rectangular waveform shown in FIG. 5 is used as a correction pulse. A pulse that drives the vertical scanning circuit is generally used as the correction pulse because the pulse has the opposite polarity and the horizontal period. The correction pulse is mixed with the output of the preamplifier using resistors 25 and 24 from the terminal 30 to remove the black level offset current I_B. Uneven offset current of the solid state image pick-up device is removed by adjusting the variable resistor 25. The period T of the correction pulse may not be coincident with the horizontal flyback period. Preferably, the period T is equal to or longer than a black level detecting period.

FIG. 10a is a circuit diagram illustrating a solid state image pick-up device according to another embodiment of the present invention. A signal output line of the solid state image pick-up device is separated by a MOS transistor 70 and a well 50 below the MOS transistor 70 is separated from a well 19 of other portion. The MOS transistor 70 is conducted during a horizontal scanning period, and performs switching by adding a rectangular waveform shown in FIG. 10b to a terminal 77 at a period T including the black level detecting period which is the horizontal flyback period. Therefore, the offset current occurs in the period T, and the black level at the horizontal scanning period can match the DC reproduction black level by

adjusting the offset current. The offset current generated at the period T can simply be adjusted by converting a voltage of the well 50 below the transistor 70 (see FIG. 8).

FIG. 11 is a circuit diagram illustrating a solid state image pick-up device according to another embodiment of the present invention. Referring to FIG. 11, horizontal scanning is performed by a charge coupled device. This is described in electronic communication society technology report (February 21, 1980) titled CCD readout type new solid state pick-up device by priming transmission:SSD79-100 in the name of terakawa et al. After the output of a charge coupled device 81 is reset by a reset transistor 85, the signal output from the charge coupled device 81 is output from a terminal 90 using two-stage source followers 84 to 87. In this embodiment, a MOS transistor 88 supplies a voltage 89 to the output of the charge coupled device 81 during a partial period T (FIG. 11b) of the horizontal flyback period. The black level of the horizontal scanning period can match the standard black level of the partial period T by adjusting the voltage 89, thereby removing offset current.

As described above, in the solid state image pick-up device according to the present invention, the black level offset current I_B can be removed and stable images can be obtained, in which black balance is not changed even if white balance is changed.

4. Brief Description of the Drawings.

FIG. 1 is a circuit diagram illustrating an example of a related art solid state image pick-up device, FIG. 2 is a timing chart of output pulses of scanning circuits of the solid state image pick-up device shown in FIG. 1, FIG. 3 is a sectional view of the solid state image pick-up device shown in FIG. 1, FIG. 4 illustrates charge transmission of the solid state image pick-up device shown in FIG. 1, FIG. 5 to FIG. 8 illustrate a waveform, a circuit, a structure, and properties of black level offset current, and FIG. 9 to FIG. 11 illustrate circuits and waveforms of the embodiment of the present invention.

15: solid state image pick-up device

20: preamplifier

40: matrix circuit

50: well of decoupling transistor

70: decoupling transistor

81: charge coupled device

82: coupling circuit

83 to 88: MOS transistor

89: power source

90: signal output terminal

91: power source

H_{BL}: horizontal flyback period

H_{SC}: horizontal scanning period

I_B: black level offset current